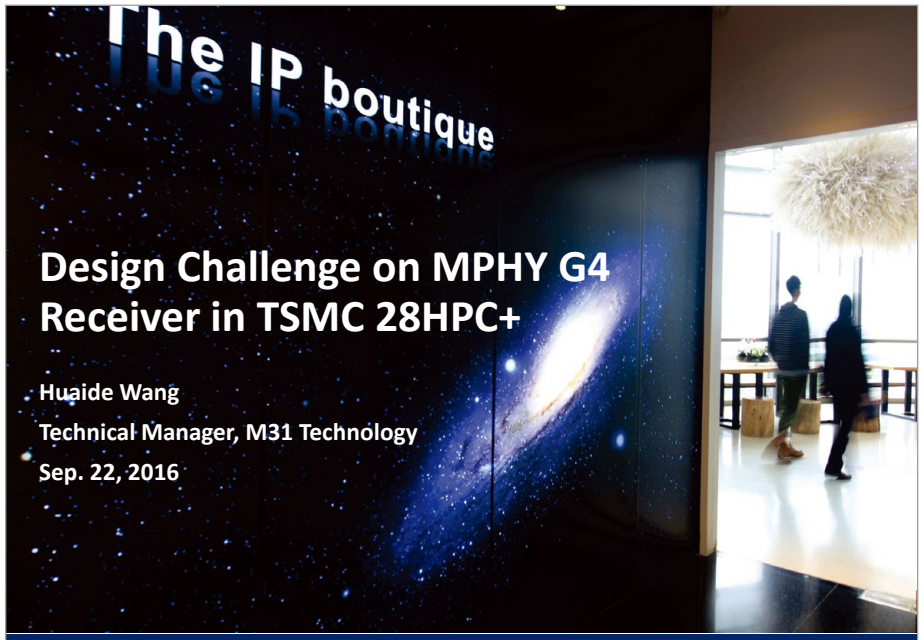
Design Challenge on MPHY G4 Receiver in TSMC 28HPC+

M31 Technology

ABSTRACT

Along with the increasing of operation speed, the system compatibility is become more sensitive with channel environment. The receiver here plays an significant role in dealing with channel ISI, return loss, and noise management. Moreover, since the serdes may not always operate at highest speed, the power scalability becomes more important in most applications.

In this presentation, we gives an overview of the impact on the receiver design from MPHY's requirement. Based on the analysis, we will introduce our receiver architecture, in which we try to get balanced in the trade-off between power, area, and circuit complexity. The simulation shows that we can achieve 9 mW/Gbps in MPHY G4 and 7 mV/Gbps in MPHY G3 in 28HPCP 1.8-IO process.



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Sep. 22, 2016

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Outline

- Wireline Development Overview
- Environment Gap between MPHY G3 and G4
- MIPI MPHY Design Technique
  - Equalization Consideration
  - Burst-Mode CDR
- Summary

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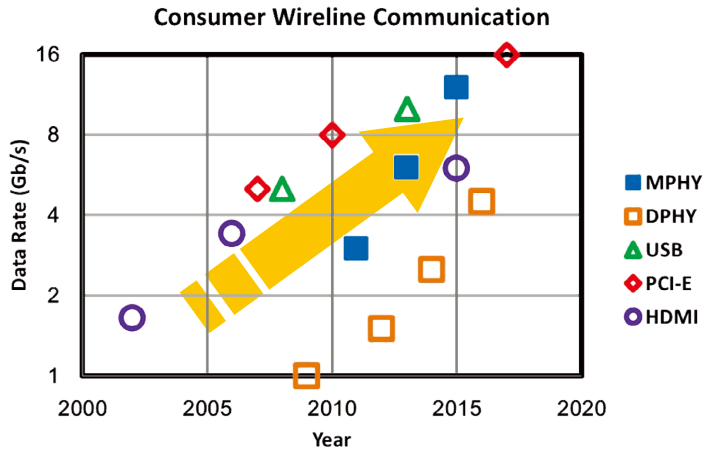
Evaluation of Wireline Standard



➔ Mobile communication speed double per 2 years.

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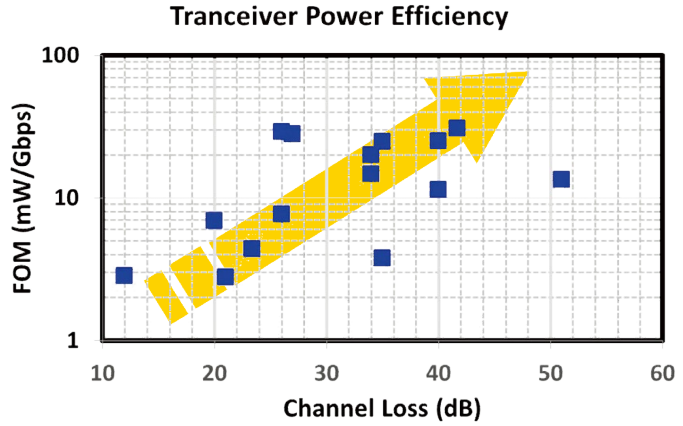
Transceiver Development Status



➔ Trend Line: 10X FOM / 20 dB Loss

[1] B. Zhang, "A 28Gb/s Multi-Standard Serial-Link Transceiver for Backplane Applications in 28nm CMOS," *ISSCC*, 2015.

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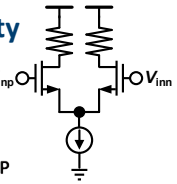
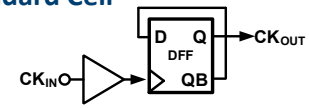
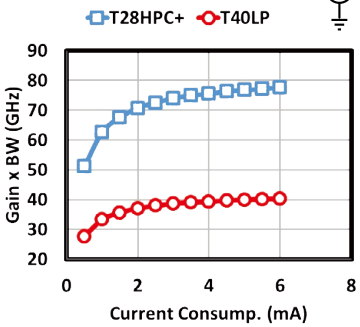
Technology Improvement

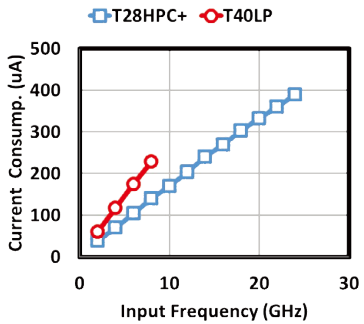
- CML Buffer Property
  - ➔ 2x GB Production



- Standard Cell







➔ It is the time to get 10-Gbps+ interface in mobile!

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Environment Gap between MPHY G3 and G4

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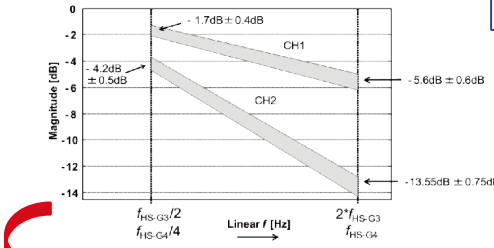
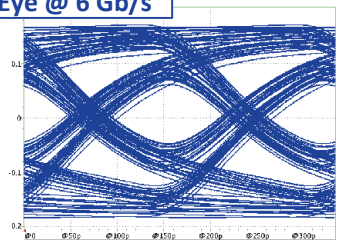
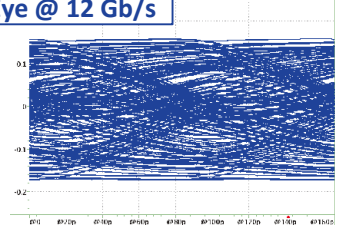
Channel Loss & ISI

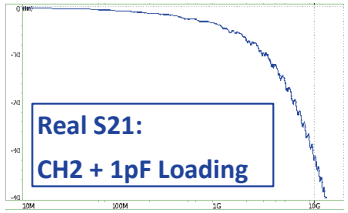


Eye @ 6 Gb/s



Eye @ 12 Gb/s





Real S21:
CH2 + 1pF Loading

➔ What makes the large difference ?

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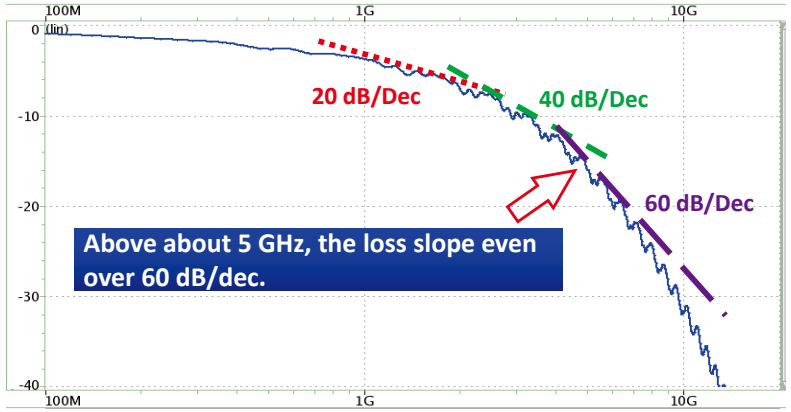
Channel Loss Curve Analysis

- Loss slope becomes sharper in higher frequencies.



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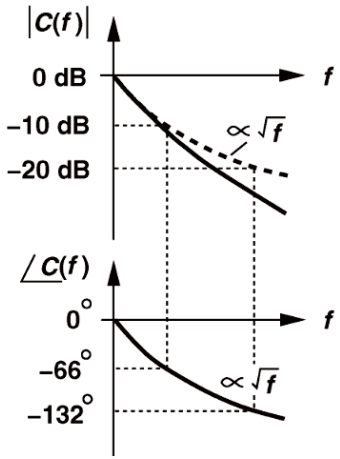
Basic Property of Channel Loss

$$C(f) = exp\left[-k_s l(1+j)\sqrt{f} - k_d l f\right]$$

- k_s: Skin effect
- k_d: Dielectric loss which appears in higher frequency

➔ Only demonstrates the 10-dB & 20-dB slope.



[2] Jri Lee, "A 20-Gb/s Adaptive Equalizer in 0.13-μm CMOS Technology," *JSSC*, 2006.

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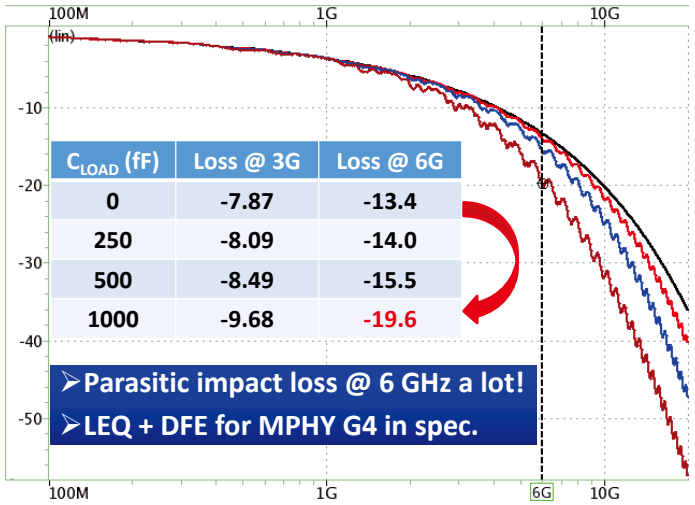
Loading Effect on Channel Loss



C_{LOAD} (fF)	Loss @ 3G	Loss @ 6G
0	-7.87	-13.4
250	-8.09	-14.0
500	-8.49	-15.5
1000	-9.68	-19.6

- Parasitic impact loss @ 6 GHz a lot!
- LEQ + DFE for MPHY G4 in spec.

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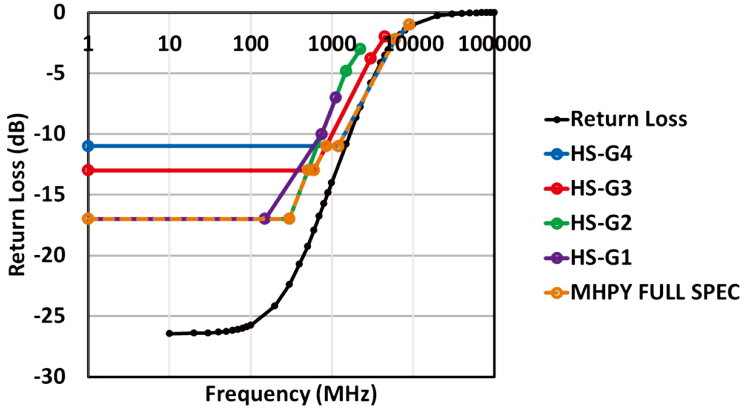
Return Loss Specification

- Loading management for return loss control.
  - MPHY from G3 to G4 : 1.7 pF ➔ 1.2pF



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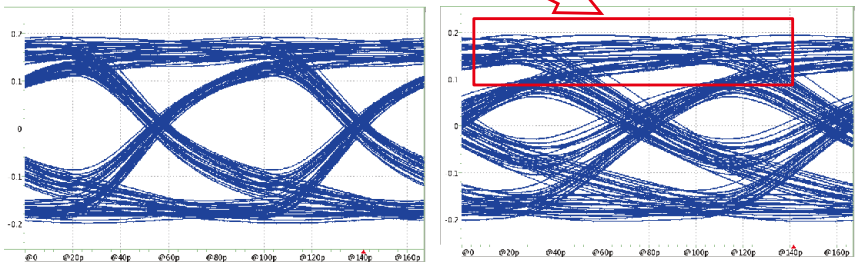
Reflection Effect

- Reflection becomes more serious in short-reach communication.
- Simulated with Reference CH1 @ 12 Gb/s

Reflection!



C_{LOAD} = 500 fF

C_{LOAD} = 1000 fF

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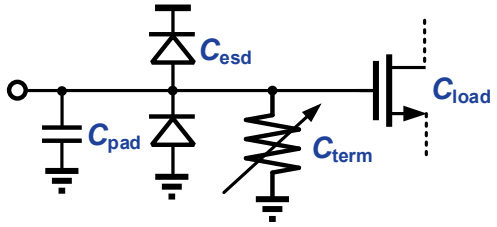
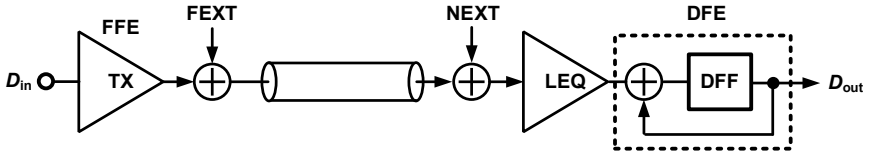
Return Loss - Loading Management

- Parasitic Source:
  - Cpad: Wirebond: 40~50 fF ⇔ Flipchip: 80~100 fF
  - Cesd: Depends on ESD spec.
  - Cterm: On-die 50-Ohm termination
    - Calibration switches bring 30~50 fF extra loading.
  - Cload: Mismatch/SNR requirement increase input MOS size.



MIPI MPHY Design Technique

Different Equalization in Link

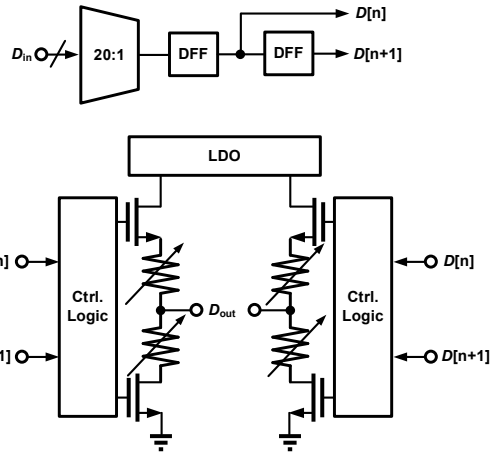


	Gain	Noise	Complexity
TX FFE	😐	🙂	☹
LEQ	🙂	☹	🙂
DFE	😐	🙂	😐

- Transmitter FFE increases driver complexity but releases LEQ dynamic range and required peaking.
- LEQ & DFE in RX has noise & power trade-off.

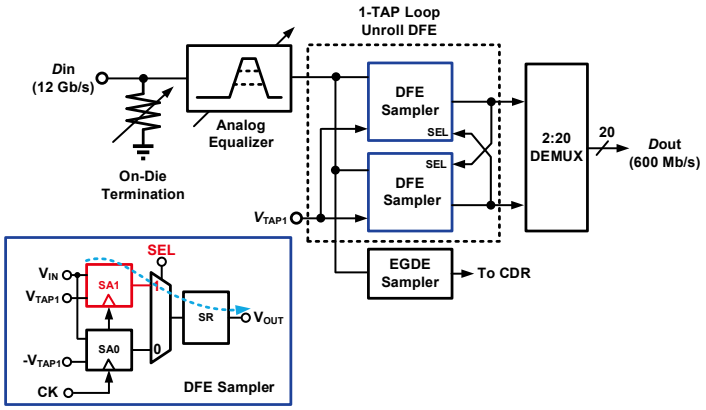
TX FFE Implementation

- Voltage-mode driver to save power.
- Challenge:
  - Programmable FFE level results in complex data logic.
  - 50-ohm calibration with FFE.

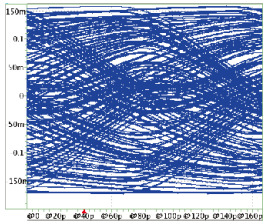


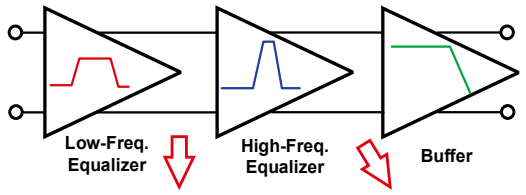
Receiver Front-End Architecture

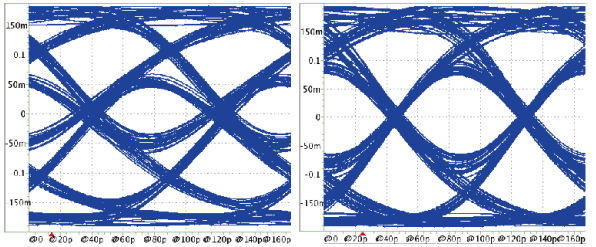
- Analog Equalizer + 1-Tap DFE.
- Half-rate architecture for power optimization.



High-Order Linear Equalizer





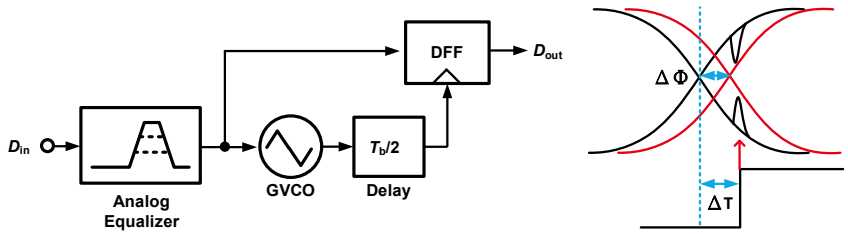


- Higher-order LEQ for better channel loss curve fitting.
- Power-scaling for different operation speed.

[3] S.Parikh, et al., "A 32Gb/s wireline receiver with a low-frequency equalizer, CTLE and 2-tap DFE in 28nm CMOS," ISSCC, 2013.]

GVCO Based Burst-Mode CDR

- Pros:
  - Fast locking time.
  - Power saving due to wide bandwidth.
- Challenge:
  - Generate 0.5-T bit delay for optimum sampling .
  - Need FLL loop to track the frequency offset .



Summary

- With the process development, power & speed hit a sweep spot that TRX below 10 mW/Gbps is ready.
- An environment gap exists to cross 10 Gb/s:
  - ISI becomes more severe from channel loss and circuit loading.
  - Reflection will be more obvious in short-reach.
- TX FFE, multi-order LEQ & 1-TAP DFE are required to overcome channel non-ideality in MPHY G4.

M31 Mobile Interface IP Status

Mobile IP Category	Proven Process	2016		2017			
		Q3	Q4	Q1	Q2	Q3	Q4
M-PHY V4.0	On-going	28 HPC+			16FFC		
M-PHY V3.0	28HPC/40LP/55LP	28 HPC+			16FFC		
D-PHY V1.2	On-going	28 HPC+			16FFC		
D-PHY V1.1	28HPC/40LP/55LP	40 ULP			28 HPC+		
C/D-PHY Combo	On-going	28 HPC+			16FFC		

➔ With TSMC 28 HPC+, we could achieve 9 mW/Gbps for MPHY G4 and 7 mW/Gbps for MPHY G3.

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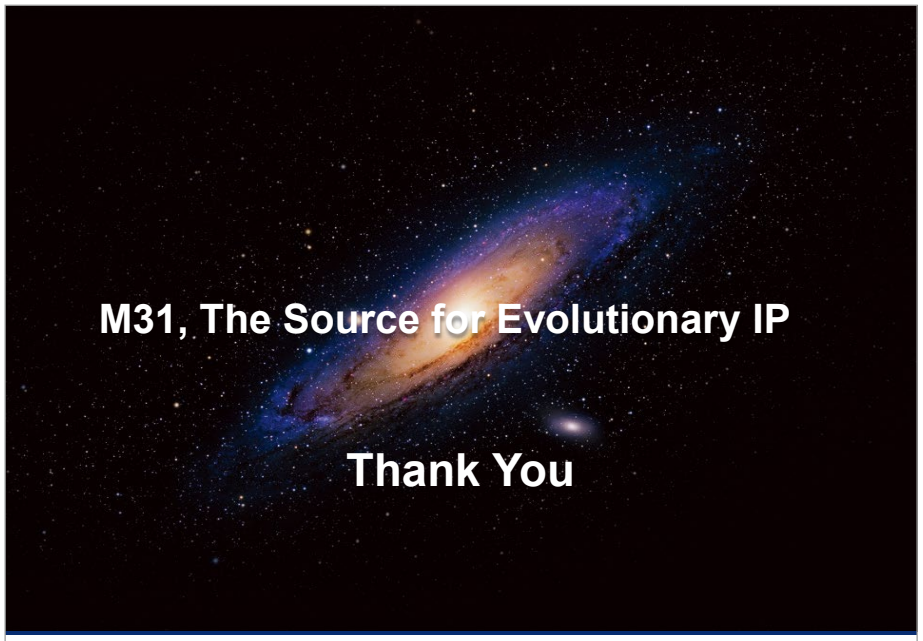

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